FIG. 1 (CONVENTIONAL ART)

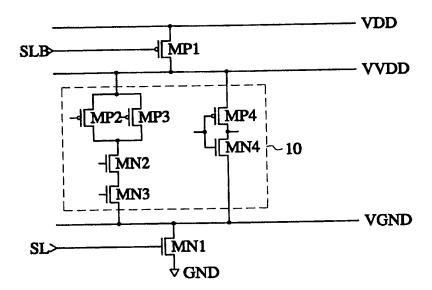
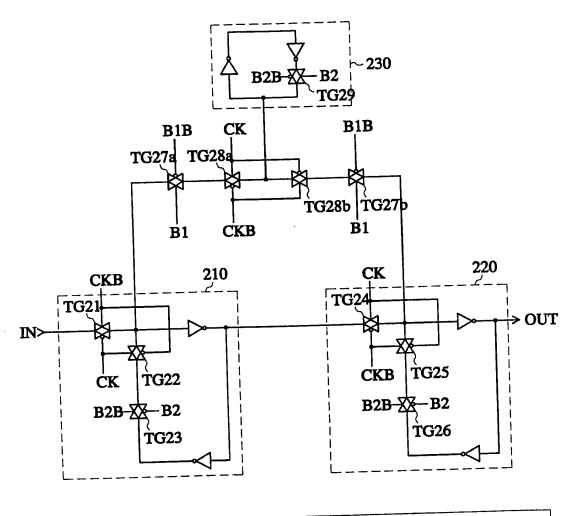


FIG. 2 (PRIOR ART)



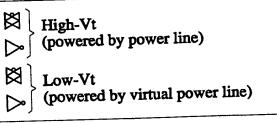
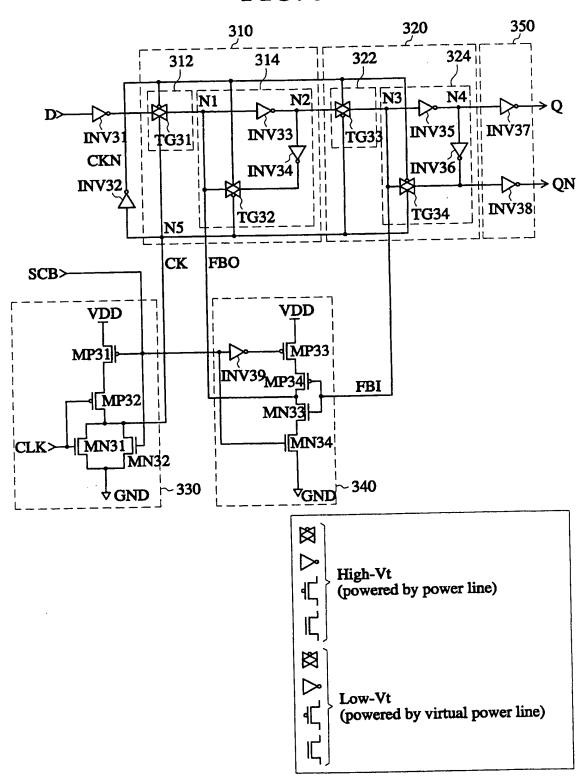


FIG. 3



4/4

FIG. 4

$$- \bigvee = - \bigvee \begin{array}{c} VDD \\ \hline \\ PMOS(high\ Vt) \\ \hline \\ VGND \end{array} \longrightarrow = - \bigvee \begin{array}{c} VDD \\ \hline \\ PMOS(low\ Vt) \\ \hline \\ VGND \end{array}$$

FIG. 5

FIG. 6

